Nanoscale CMOS and Beyond:
Negative Capacitance FETs

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Outline

- **Reminder: steep subthreshold slope: device categorization**
- **Negative Capacitance as Next Technology Booster for Computation near 100mV**
  - Negative Capacitance FETs
  - Negative Capacitance Tunnel FETs
- Conclusion

Subthrehold Slope Scaling

- Re-engineering the slope of the FET

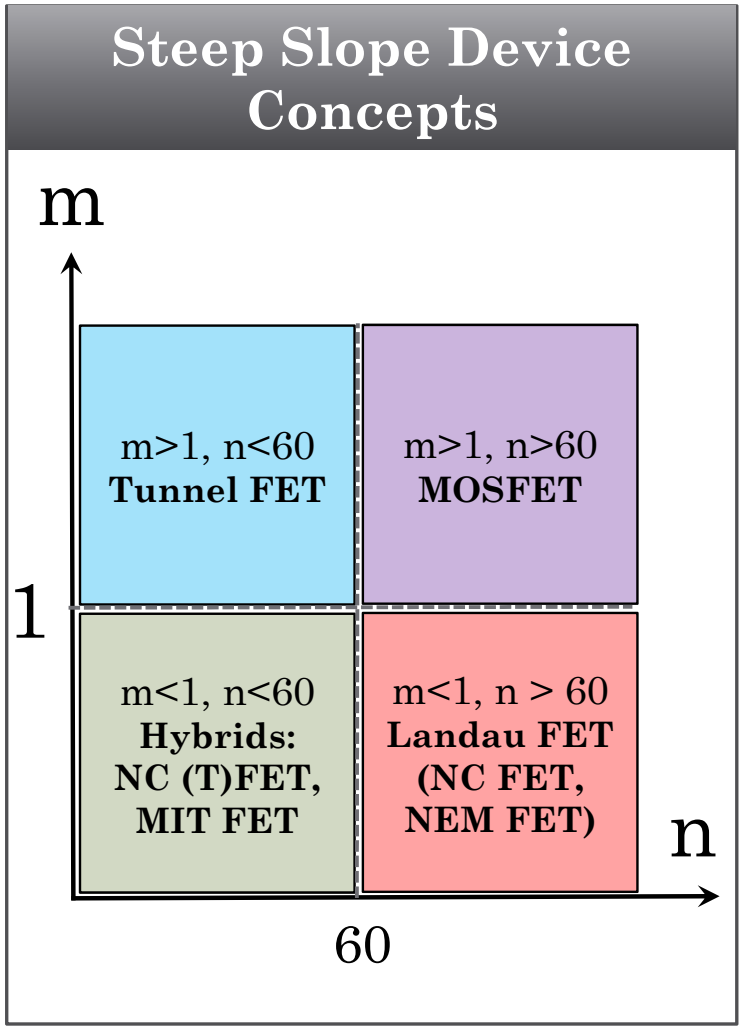
$$S = \frac{\partial V_g}{\partial(\log I_d)} = \underbrace{\frac{\partial V_g}{\partial \psi_S}}_{m}\underbrace{\frac{\partial \psi_S}{\partial(\log I_D)}}_{n} = (1+\frac{C_s}{C_{ins}})\frac{kT}{q}\ln 10 = m \times n$$

- ***Steep (subthermionic) slope:***

  m < 1 *and/or*

  n < kT/q ln10 = 60mV/dec @ RT

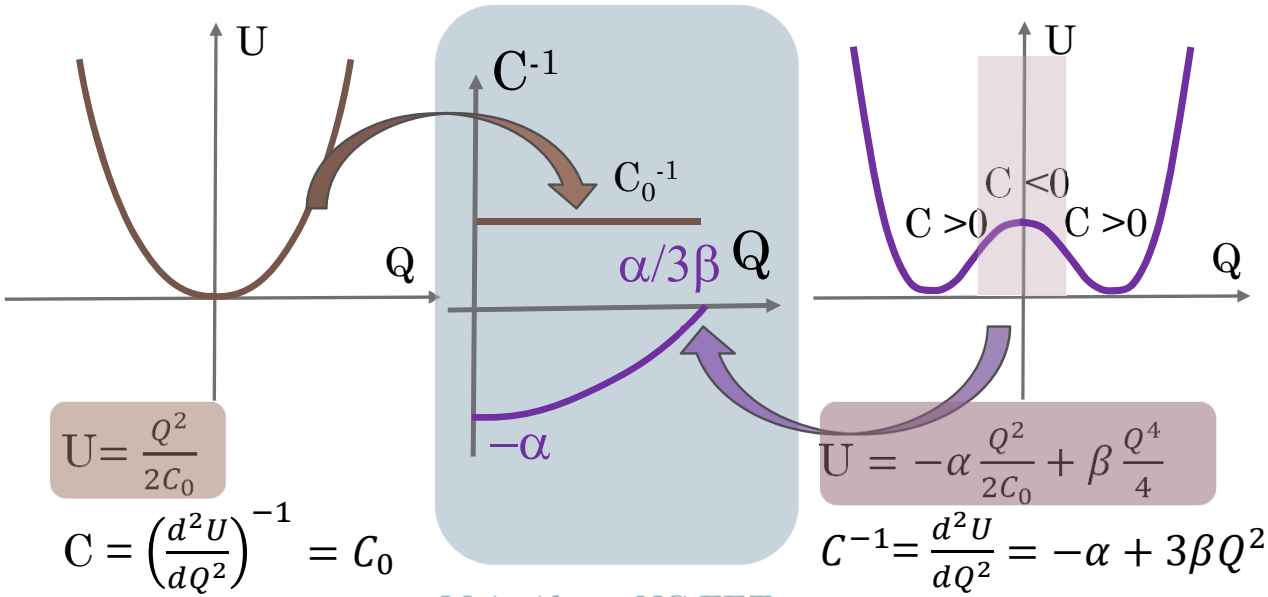
  by new physics and new device architecture.



Field Effect Transistors with Active Gates: Landau Switches

- **The *energy landscape* defines the sign of the capacitance**

Positive Capacitance | **Negative Capacitance**



$$U = \frac{Q^2}{2C_0}$$

$$C = \left(\frac{d^2U}{dQ^2}\right)^{-1} = C_0$$

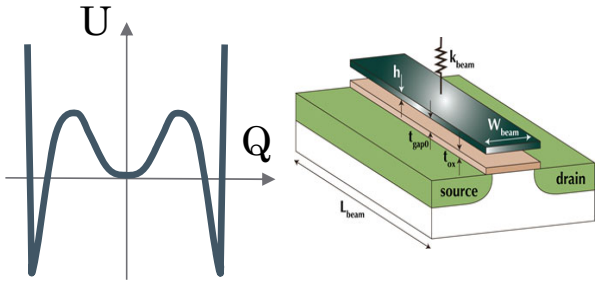
$$U = -\alpha\frac{Q^2}{2C_0} + \beta\frac{Q^4}{4}$$

$$C^{-1} = \frac{d^2U}{dQ^2} = -\alpha + 3\beta Q^2$$

M.A. Alam, NC FET, https://nanohub.org/

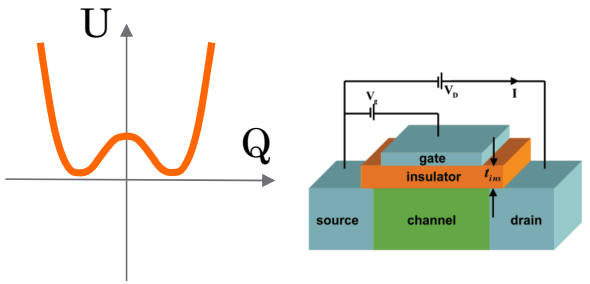
Negative Capacitance Devices

NEM FETs



N. Abelé et al., IEDM 2005.
H. Kam et al., IEDM 2005.

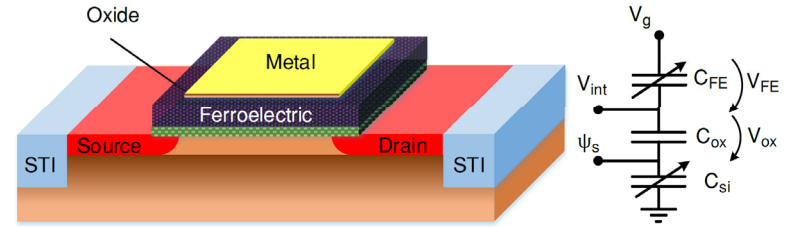
Ferroelectric NC FET



Salahuddin & Datta, Nanolett., 2008.

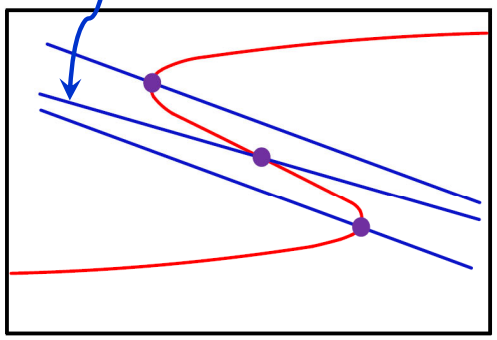
Negative capacitance in ferroelectric FETs

- Designing a good charge line & stabilized stack.

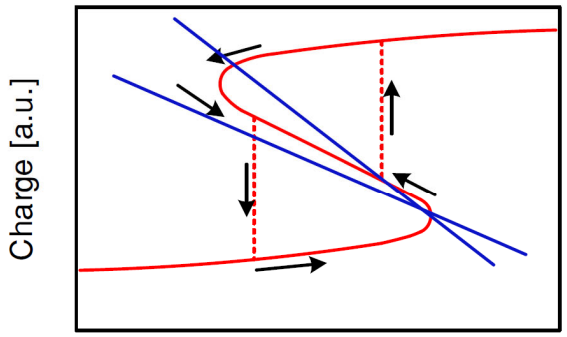


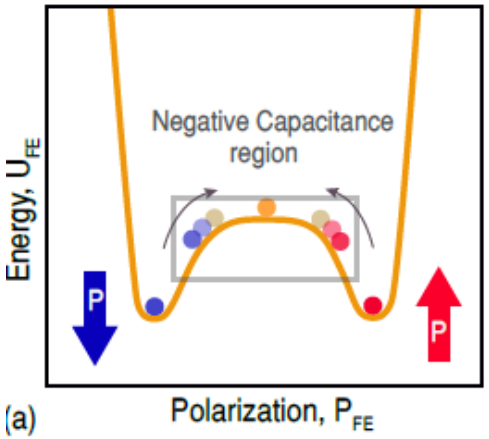
$$P = \epsilon_0 k_{ox} \frac{V_g}{t_{ox}} - E_{FE} t_{Ee} \epsilon_0 \left(\frac{1}{t_{FE}} + \frac{k_{ox}}{t_{ox}}\right) - \frac{\epsilon_0 k_{ox}}{t_{ox}} \psi_s$$

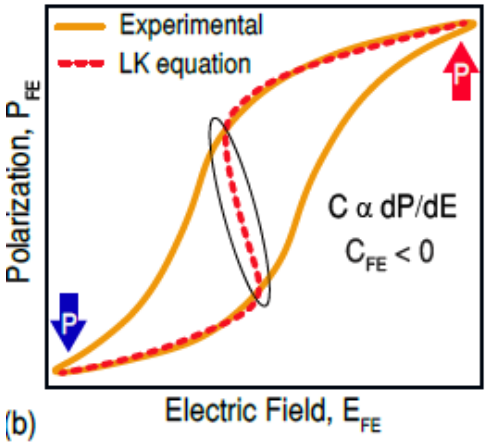
Non-hysteretic



Hysteretic

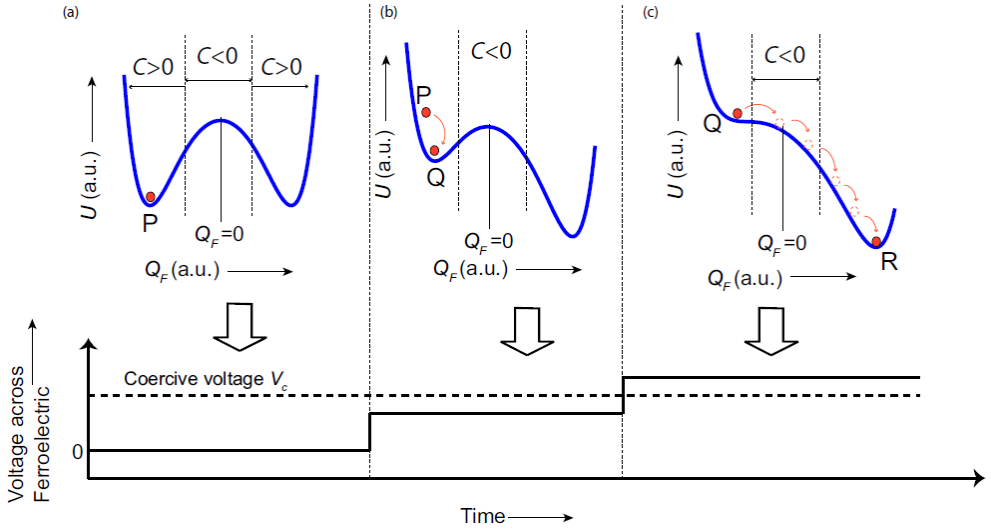






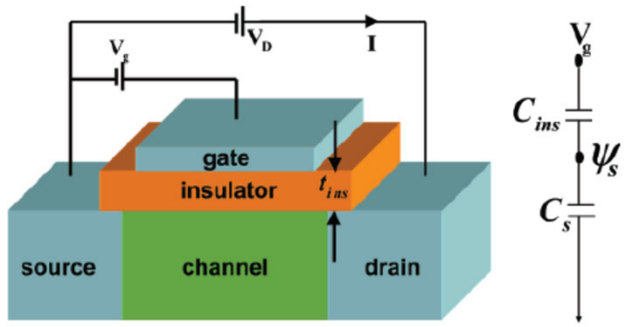
Negative Capacitance in ferroelectrics: principle (2)

- The **small signal concept-capacitance C at a given charge Q_F** is related to the potential energy U by the relation $C=[d^2U/dQ_F^2]^{-1}$
- Important: 'negative capacitance' refers to 'negative differential capacitance'.
- For a ferroelectric material, **the capacitance is negative only in the barrier region around $Q_F=0$**. Starting from an initial state P, as a voltage is applied across the ferroelectric capacitor, the energy landscape U is tilted and the polarization will move to the nearest local minimum.



Negative Capacitance in ferroelectrics: principle (1)

- **Step-up voltage transformer** to internally amplify the gate voltage, leading to values of S lower than 60mV/dec.
- Exploits a ferroelectric gate-stack FET: the negative capacitance should be stabilized, as it is an instable region of operation.



Goal: body factor, m < 1 by C_{ins} <0

$$m = \left[\frac{d\Psi_S}{dV_g}\right]^{-1} = 1 + \frac{C_s(V_g)}{C_{ins}(V_g)} < 1$$

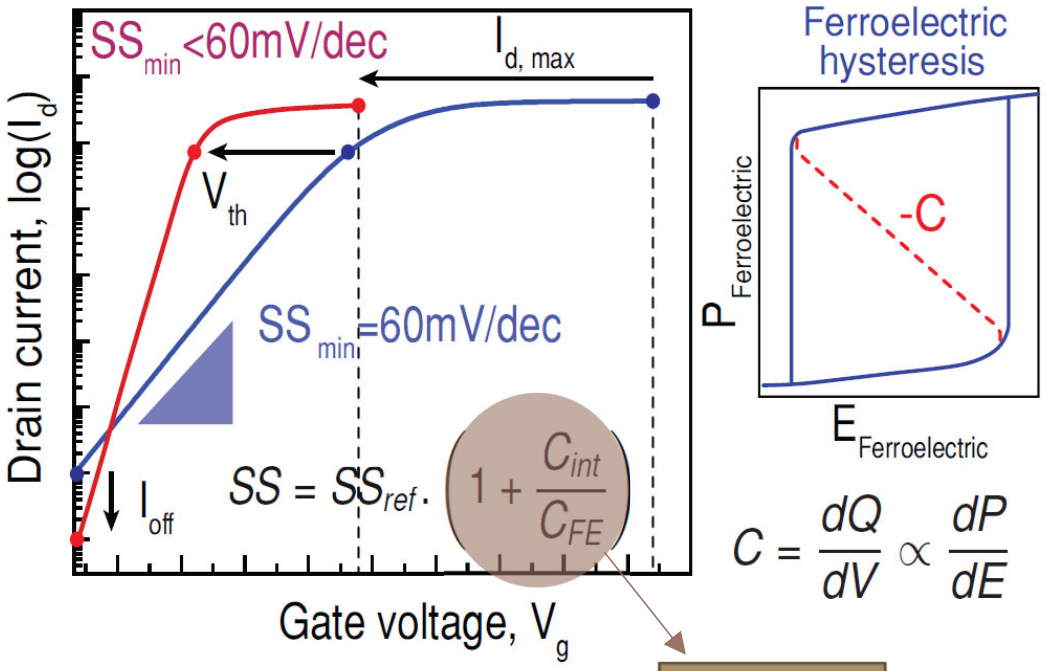
Sallahuddin & Datta, Nanoletters, 2008.

Negative Capacitance as *Additive Performance Booster* for Field Effect Transistors

Sub-1 body factor by negative capacitance:

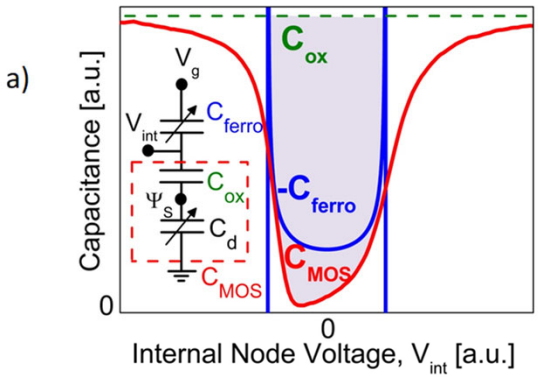
- Ferroelectric gate stack
- Reduced V_{th}
- Improved overdrive
- Steeper slope

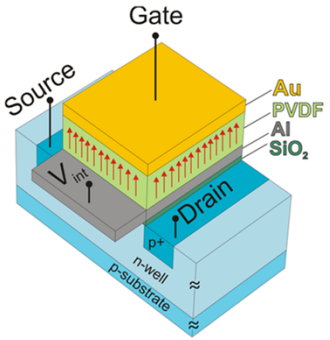
Additive technology booster on any type of Field Effect Transistor.

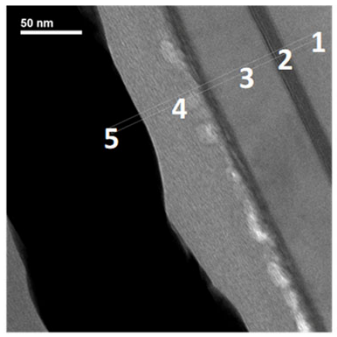


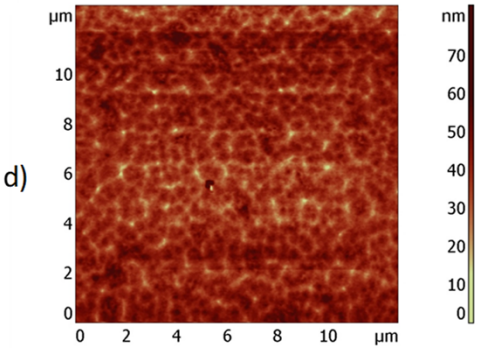
A. Saeidi et al, IEEE EDL 2017.

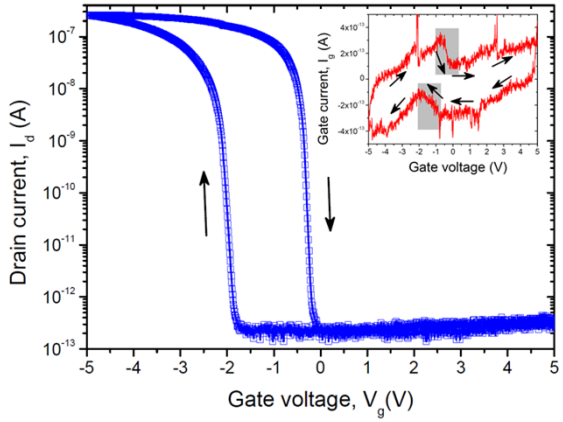
First experimental results

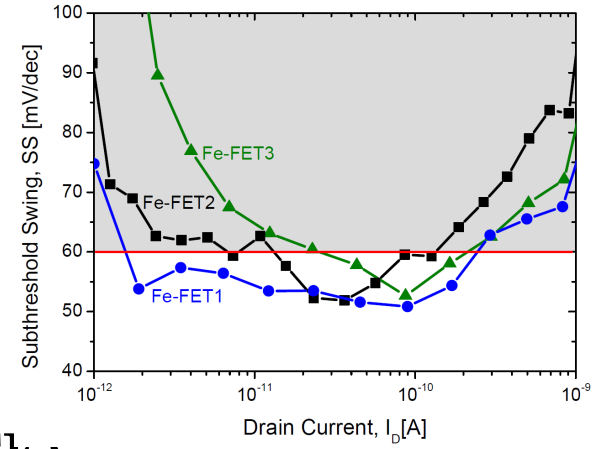










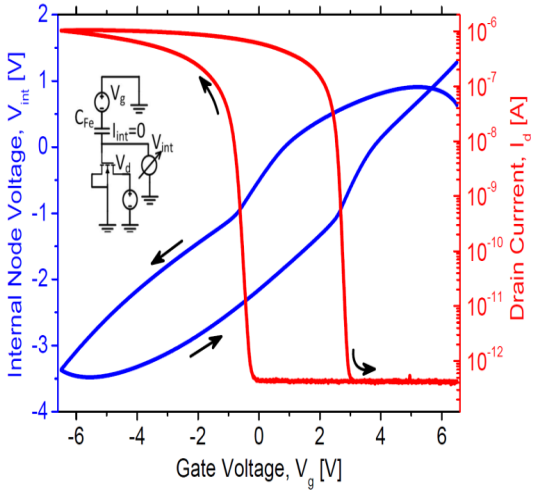


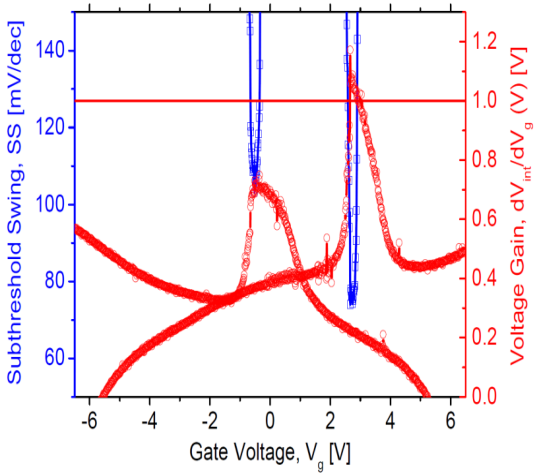
Ferroelectric organic copolymer P(VDF-TrFE)

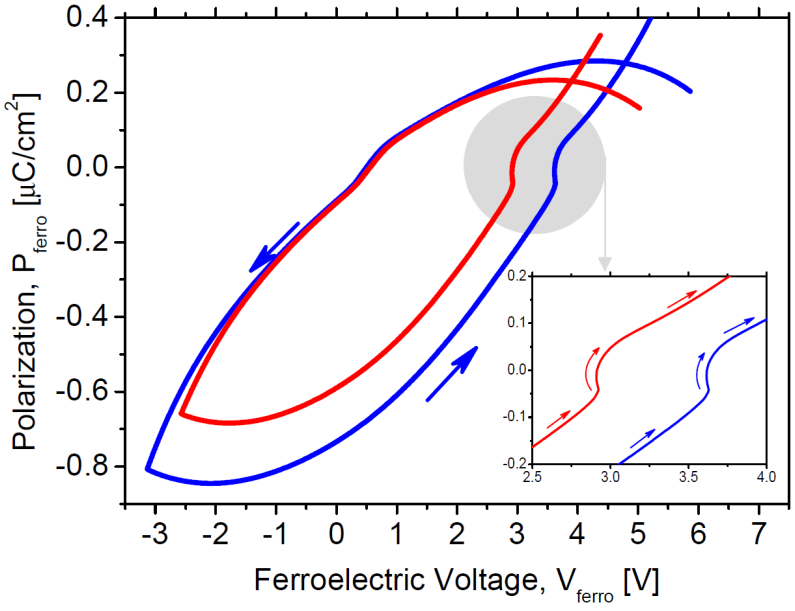
Advantages: ultra-low leakage, medium-k organic dielectric, low temperature processing
Disadvantages: slow response of dipoles (>0.5µs), thickness difficult to scale below 10nm

Signature: S-shape polarization

- **The region with voltage gain > 1 (and reduction of subthreshold swing) corresponds to the S-shape region of the P-V_{ferro} where the negative capacitance effects occurs.**

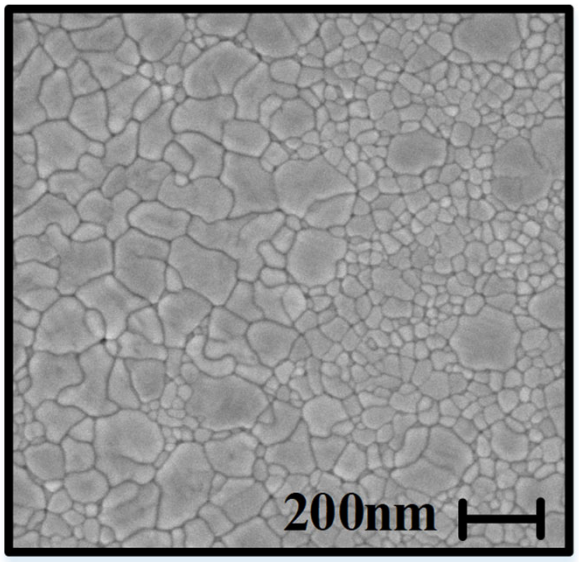


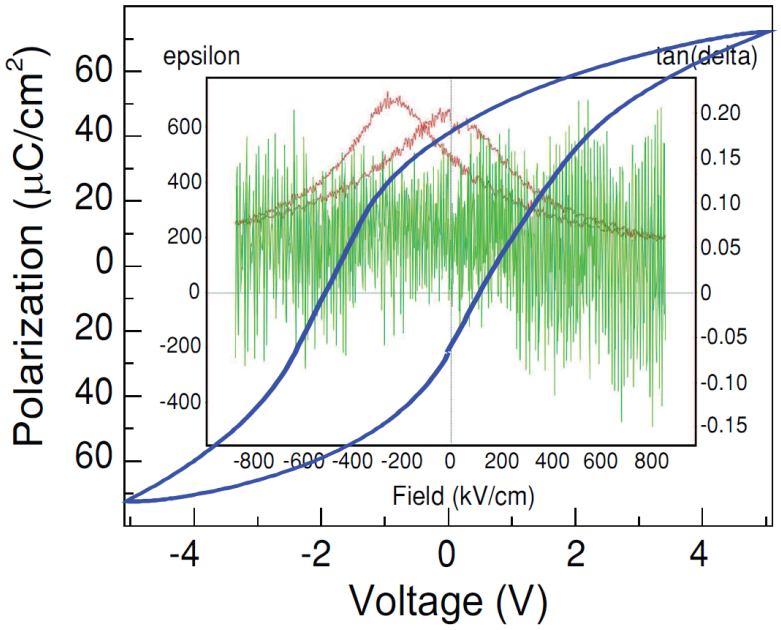




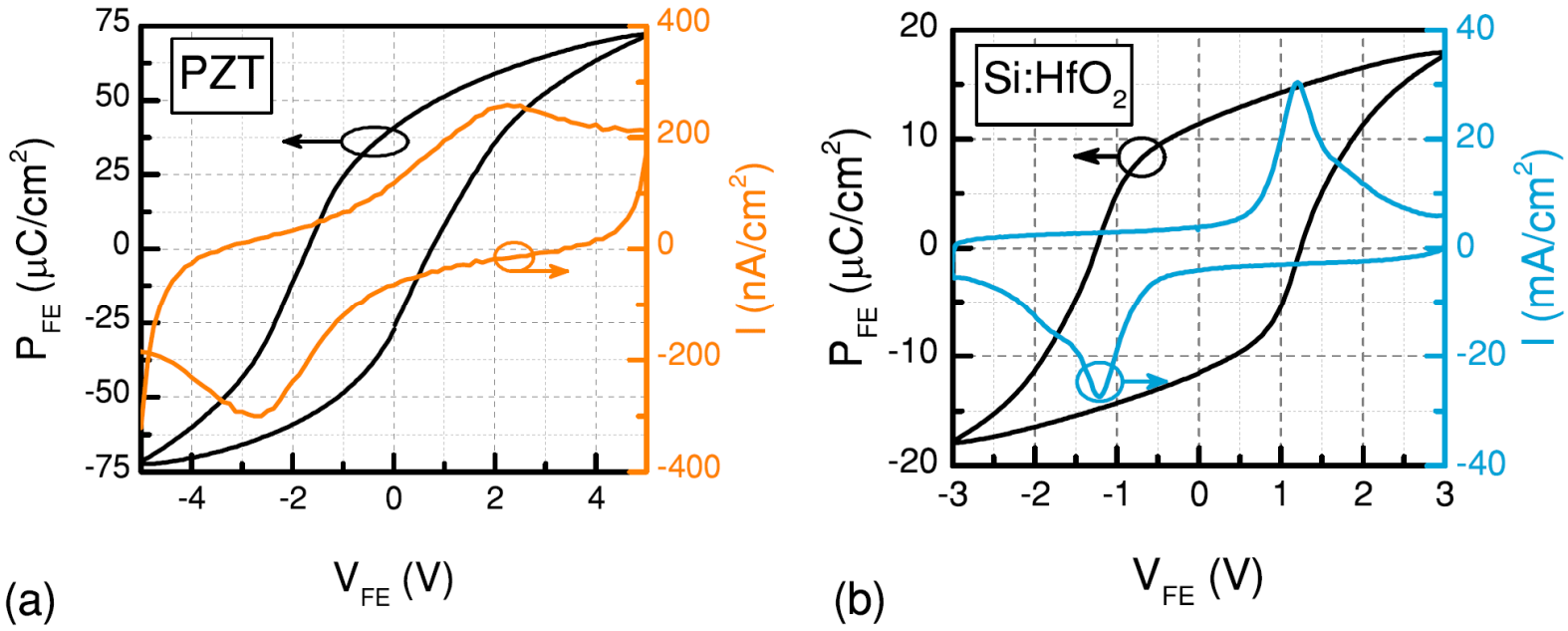
PZT as inorganic ferroelectric

- 50nm of **$Pb(Zr_{43},Ti_{57})O_3$ (PZT) ferroelectric** film grown by chemical solution deposition root on a TiO2(2nm)/Pt(100nm)/TiO2/Ti/SiO2/Si substrate
- Polycrystalline: ferrolectric multi-domains!
- Relative permittivity, coercive field, and remanent polarization: 220 – 240, 260kV/cm, and 32μC/cm^2





Ferroelectricity: PZT versus Si:HfO2

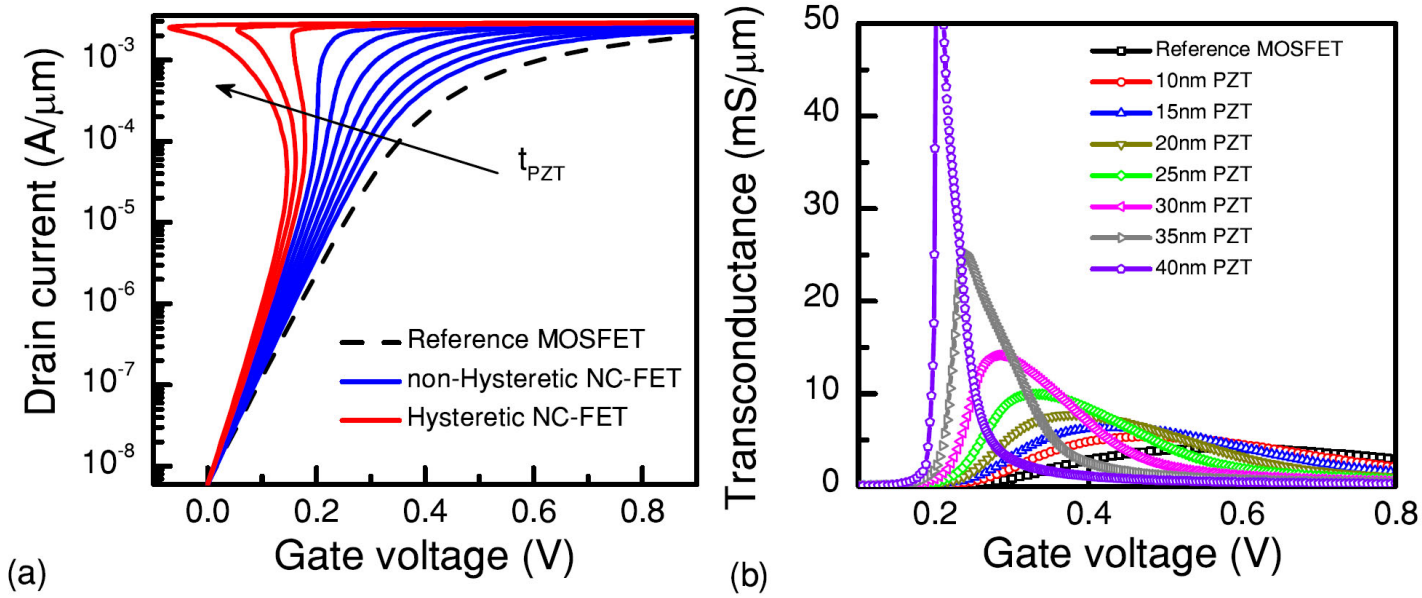


a) Polarization and current characteristics of the 46 nm thick PZT capacitor. A coercive field of +80 kV/cm; -260 kV/cm and a remanent polarization of ±30 μC/cm2 is measured. Very low leakage current, in the order of nA/cm2.

b) P-V and I-V characteristics of a silicon-doped HfO2 ferroelectric capacitor with a thickness of 15 nm and a Si concentration of 4.3%. The coercive field of ±1 MV/cm and a remanent polarization of about ±15 μC/cm2 are extracted together with a relatively higher switching current.

NC as surface potential 'amplifier'

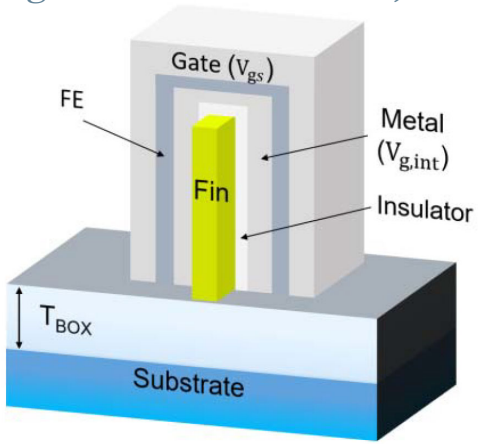
- Calibrated simulations (PZT gate stack): NC influence on the MOSFET surface potential, internal voltage gain, transfer characteristics and transconductance (weak to strong inversion)

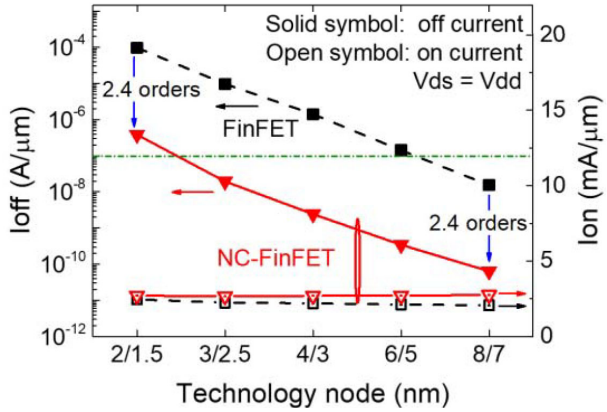


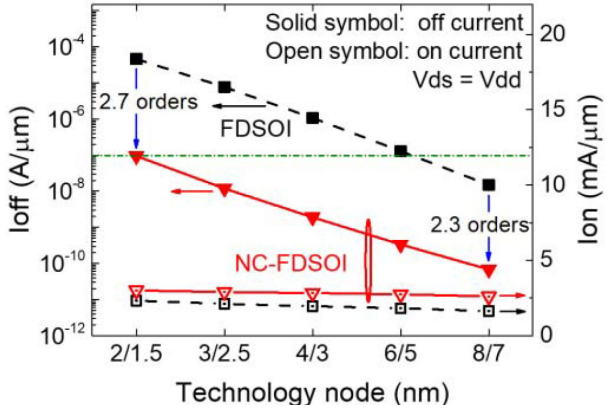
NC as technology booster enabling 2nm MOSFETs

- Predictive simulation
- NC is effective of both FinFETs and UTB SOI FETs
- Significantly improved Ioff
- Better or preserved Ion
- Improved roll-off and DIBL
- *More data on dynamic regime needed*

V. Hu et al., Negative Capacitance enables FinFET and FDSOI scaling down to 2nm node, IEDM 2017.

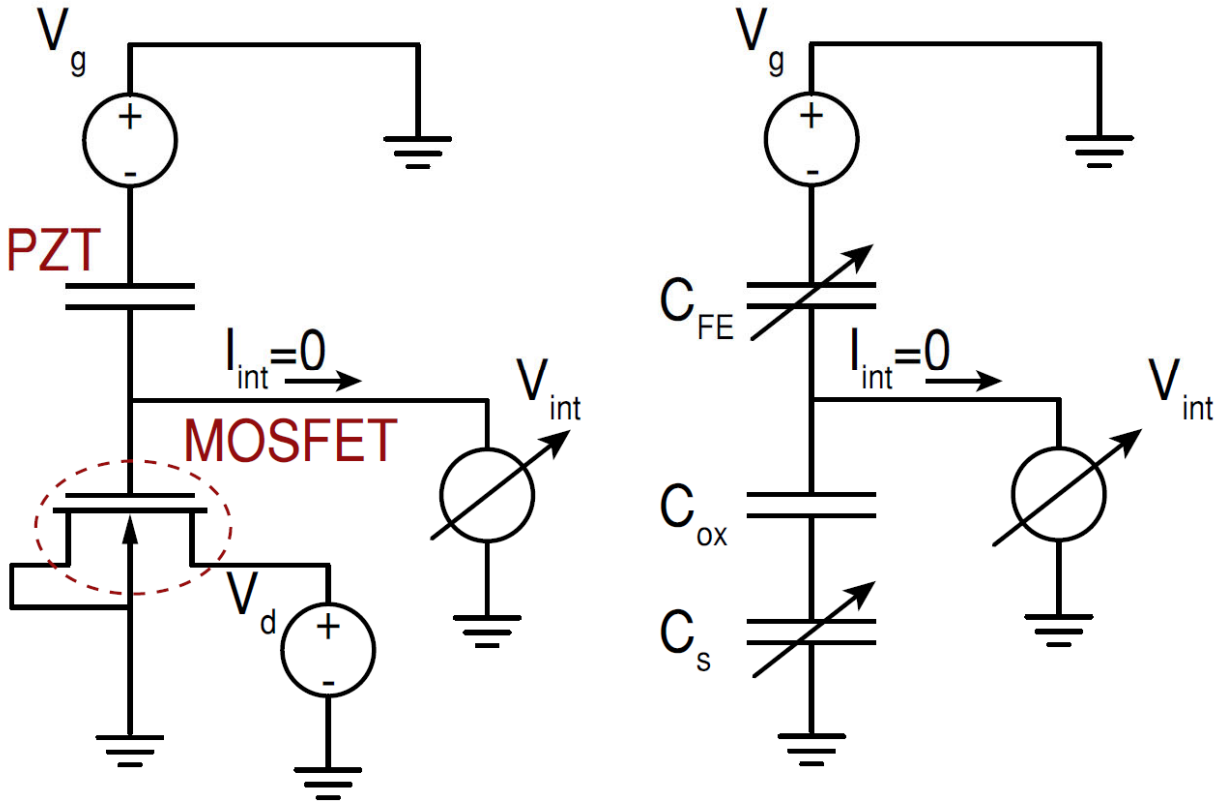






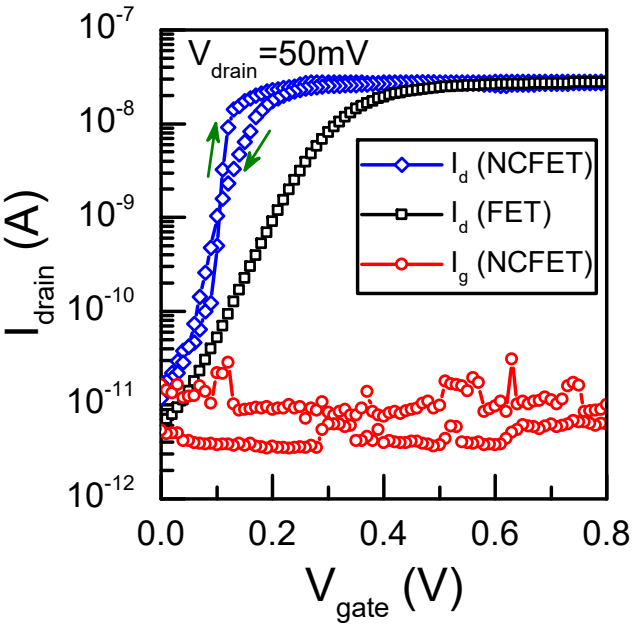
Electrical characteristics	Ioff (A/μm)		Ion (mA/μm)		Vt,sat (V)		SS (mV/dec)	
Technology node (nm)	3/2.5	2/1.5	3/2.5	2/1.5	3/2.5	2/1.5	3/2.5	2/1.5
NC-FinFET	1.95E-8	3.82E-7	2.67	2.71	0.233	0.159	76	91
FinFET	9.63E-6	9.69E-5	2.25	2.47	0.015	-0.154	132	236
NC-FDSOI	1.2E-8	9.44E-8	2.9	3.01	0.267	0.226	84	98
FDSOI	7.68E-6	4.56E-5	2.12	2.33	0.031	-0.093	147	208

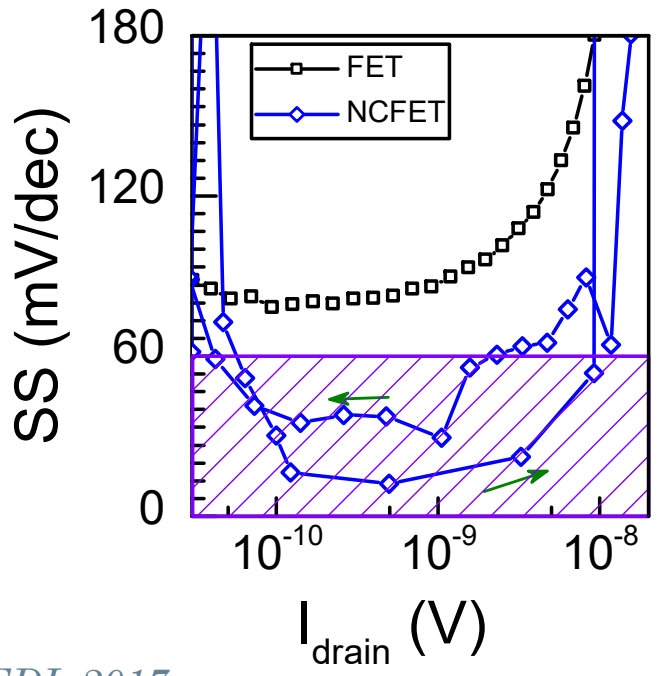
NC FD SOI MOSFETs + PZT capacitors: experiments

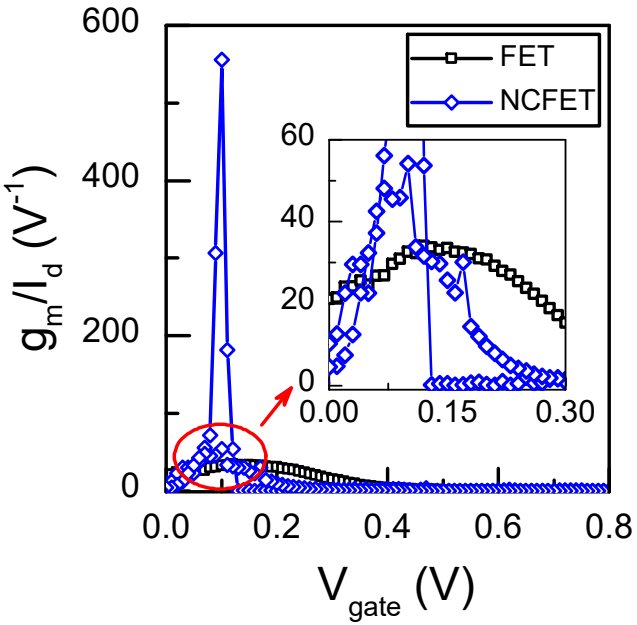


Quasi non-hysteretic NC FD SOI n-type MOSFET: experiments

Overdrive ~0.2V **Swing : 3.5 (20mV/dec)** **g_{max} x 20**



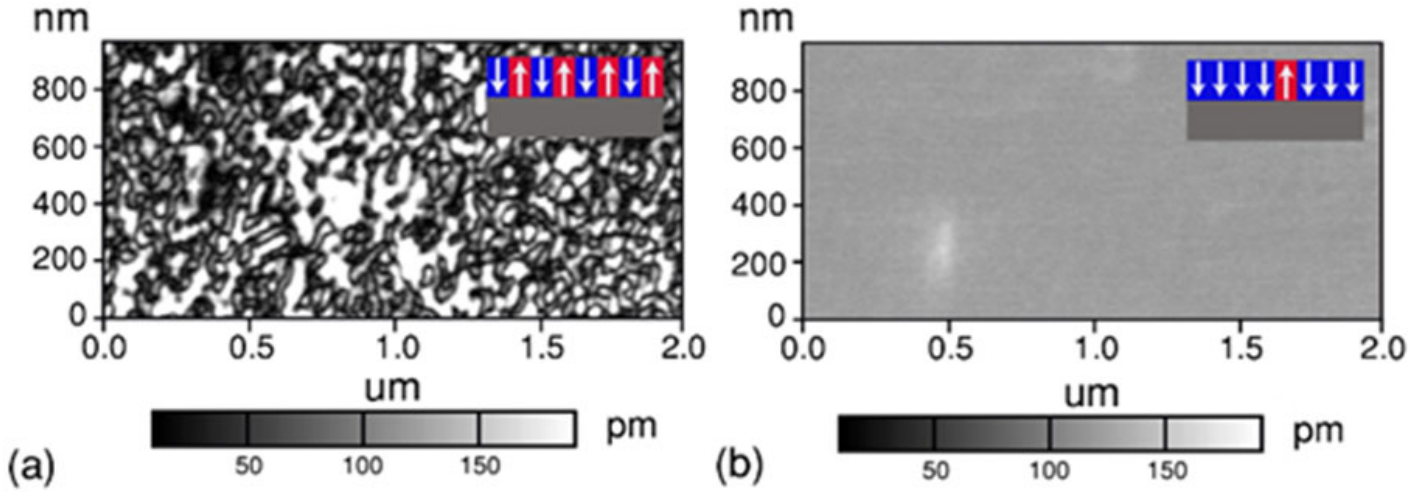




A. Saeidi et al, IEEE EDL 2017.

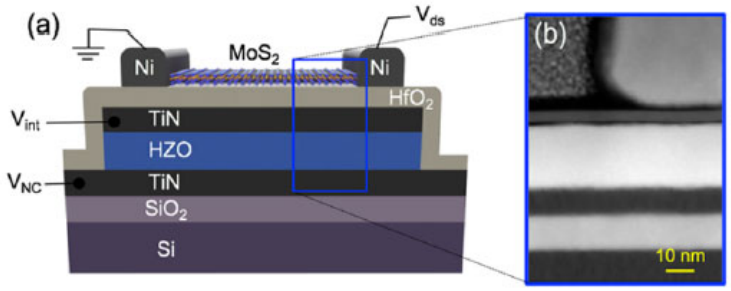
Limits of polycrystalline NC PZT capacitors: voltage training needed

- 46 nm of PZT with 43/57 (Zr/Ti) ratio is deposited on a stack of TiO2(2 nm)/Pt(100 nm)/TiO2/Ti/SiO2/Si by employing the sputtering technique
- Training of PZT capacitors: ***multi-domain*** *trained to* ***single-domain ferroelectric***

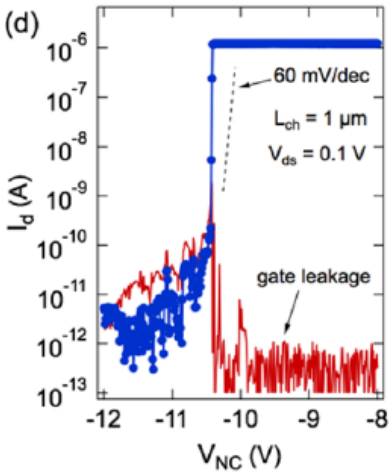


Piezoelectric response of the PZT ferroelectric thin film (PFM measurement).
(a) Before training: broad distribution of nucleation energies and coercive fields
(b) After training: single-domain behavior of poled PZT layer (20 cycles at ±7V).

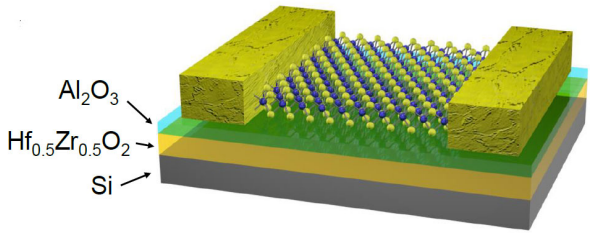
Negative Capacitance in HZO gives 2D Transistors a Positive Performance Boost

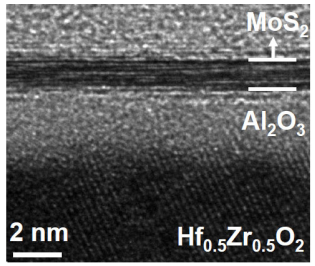


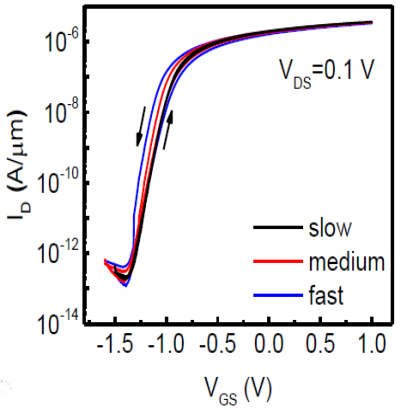
F. A. McGuire, Nano Lett. 2017.

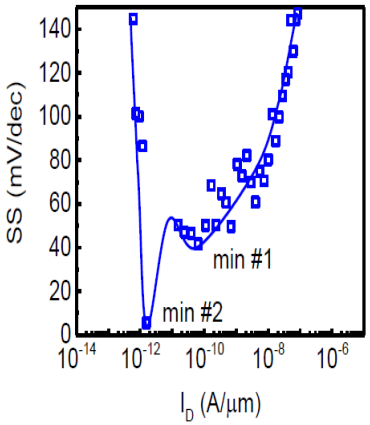


Steep Slope NC MoS2 Transistors





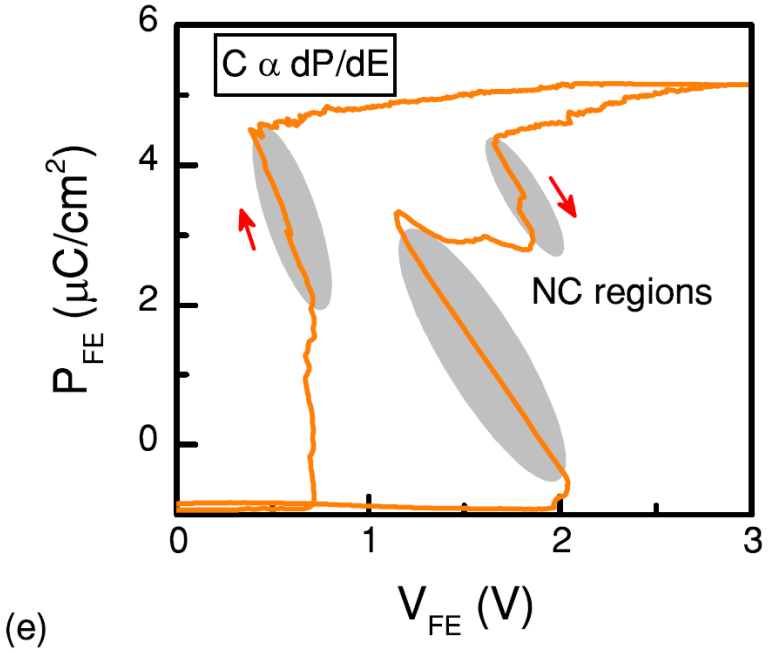




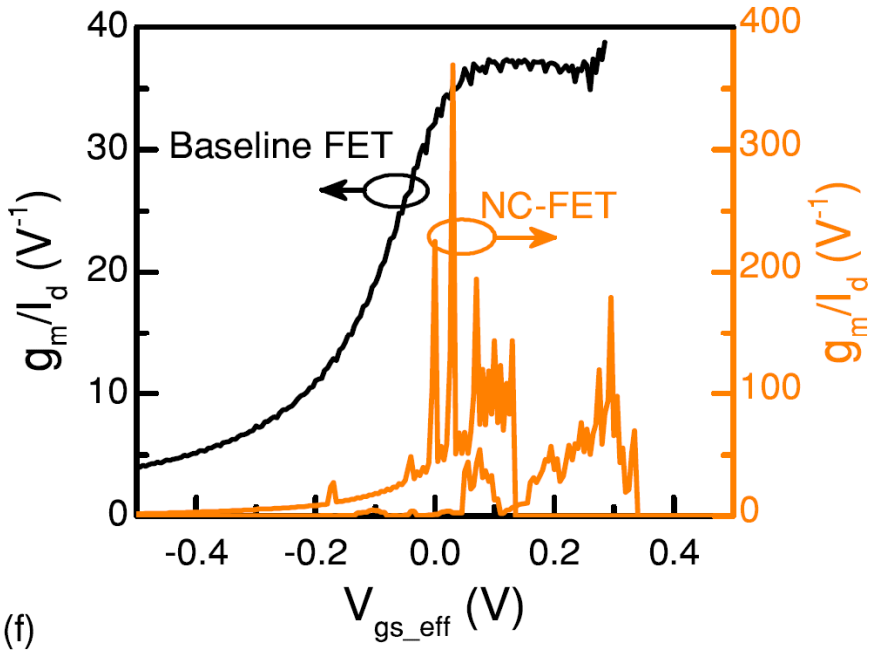
M. Si et al., arXiv.org, 2017.

P-type NC MOSFETs

- Negative Capacitance as booster of digital and analog performance of both n- and p-type MOSFETs needed for complementary logic
- Similar PZT matched capacitors as in previous experiments (~10 x 10 um^2)



(e)

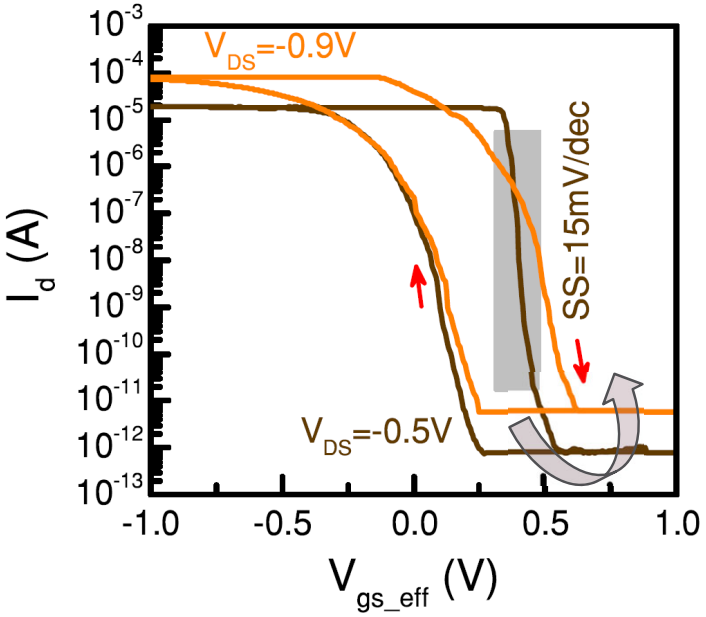


(f)

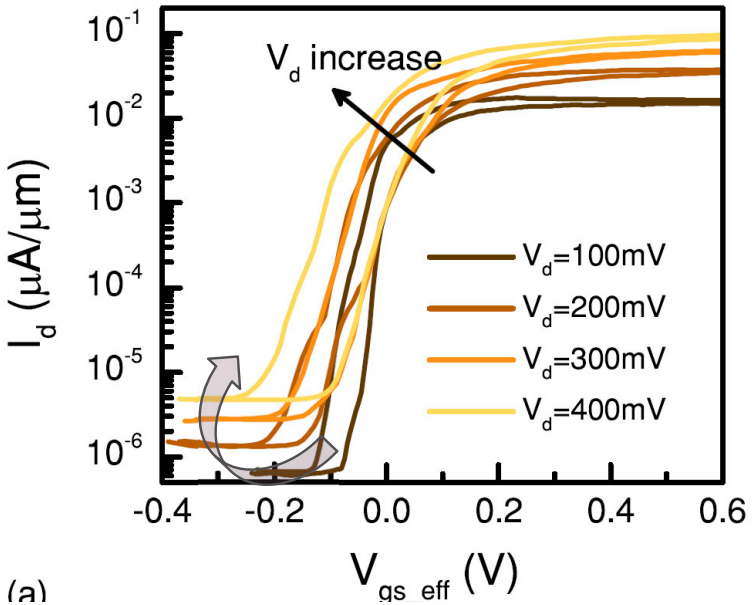
Effect of drain-to-source voltage on NC effect and internal voltage gain

- Internal voltage gain is reduced
- Swing is increased at low currents
- Leakage floor is increased

p-type NC (PZT) MOSFET



n-type NC (Si:HfO2) MOSFET



(a)

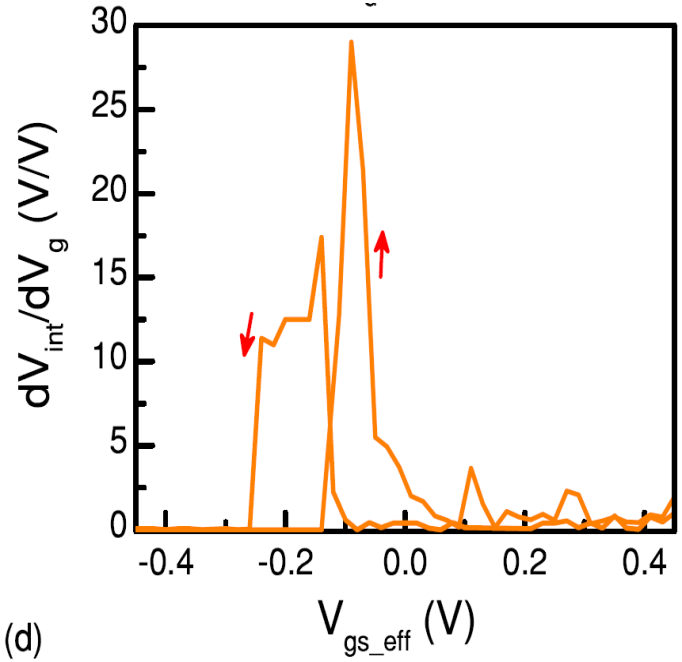
Small Hysteresis NC n-MOSFETs

- Capacitance matching over large region of operation

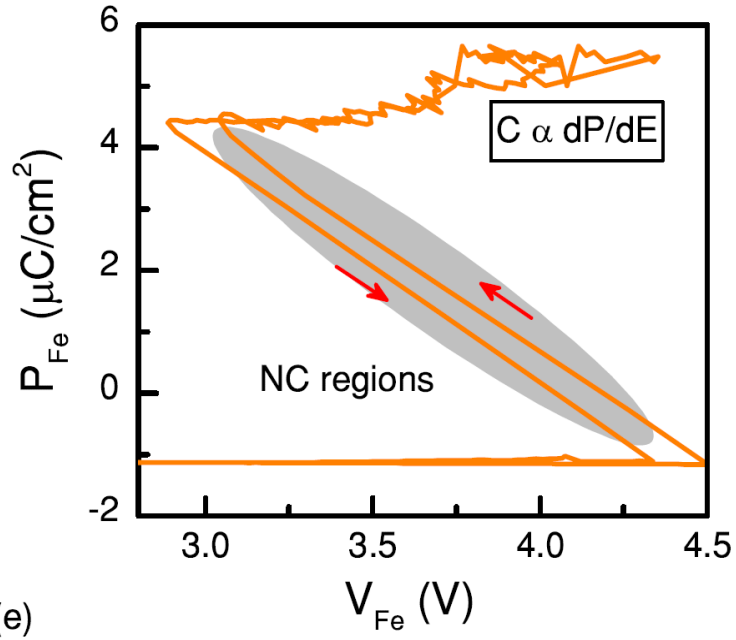
$$SS_{NC}=(\frac{\partial LogI_d}{\partial V_g})^{-1}=\frac{\partial V_{int}}{\partial LogI_d}\times\frac{\partial V_g}{\partial V_{int}}=\frac{SS_{ref}}{\beta}.$$

$$\beta=\partial V_{int}/\partial V_g=C_{FE}/(C_{FE}+C_{int}).$$

$$C_{total}^{-1}=C_{FE}^{-1}+C_{int}^{-1}>0.$$



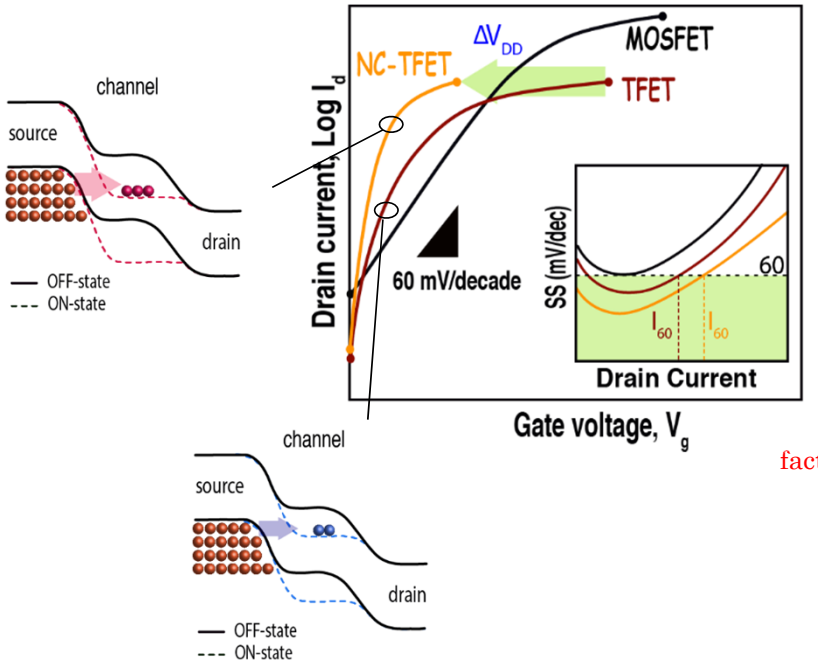
(d)



(e)

NC-TFET: Device concept

- An effective **NC enhances the tunneling probability at lower gate voltages**



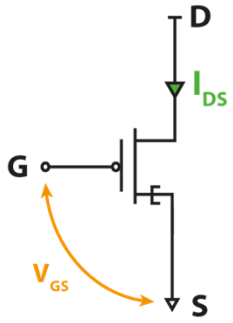
Thermal injection limit

$$n = \frac{d\Psi_S}{d(\log_{10} I_{DS})}$$

Body factor limit

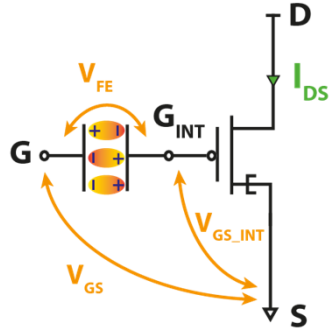
$$m = \frac{dV_{GS}}{d\Psi_S}$$

TFET



< 60 mV/dec

NC-TFET



< 60 mV/dec

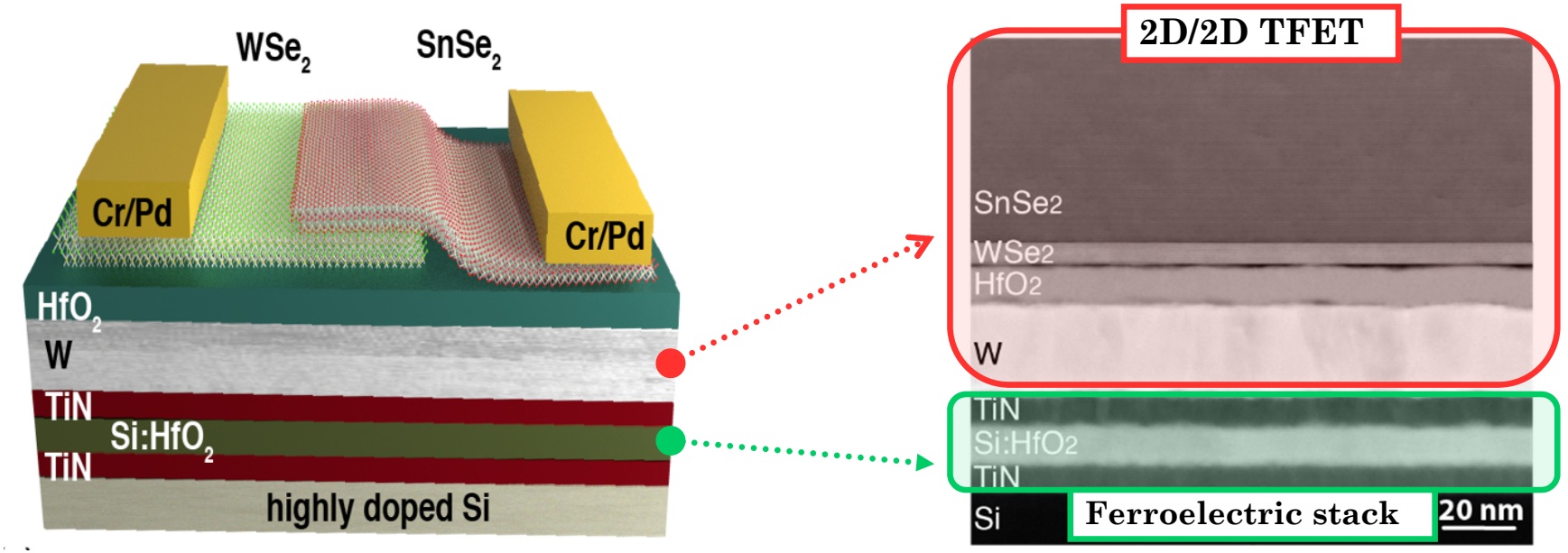
$$1 + \frac{C_d}{C_{ox}} > 1$$

$$\frac{dV_{GS}}{dV_{GS\_INT}} \cdot \frac{dV_{GS\_INT}}{d\Psi_S}$$

$$1 + \frac{C_d}{C_{ox}} > 1$$

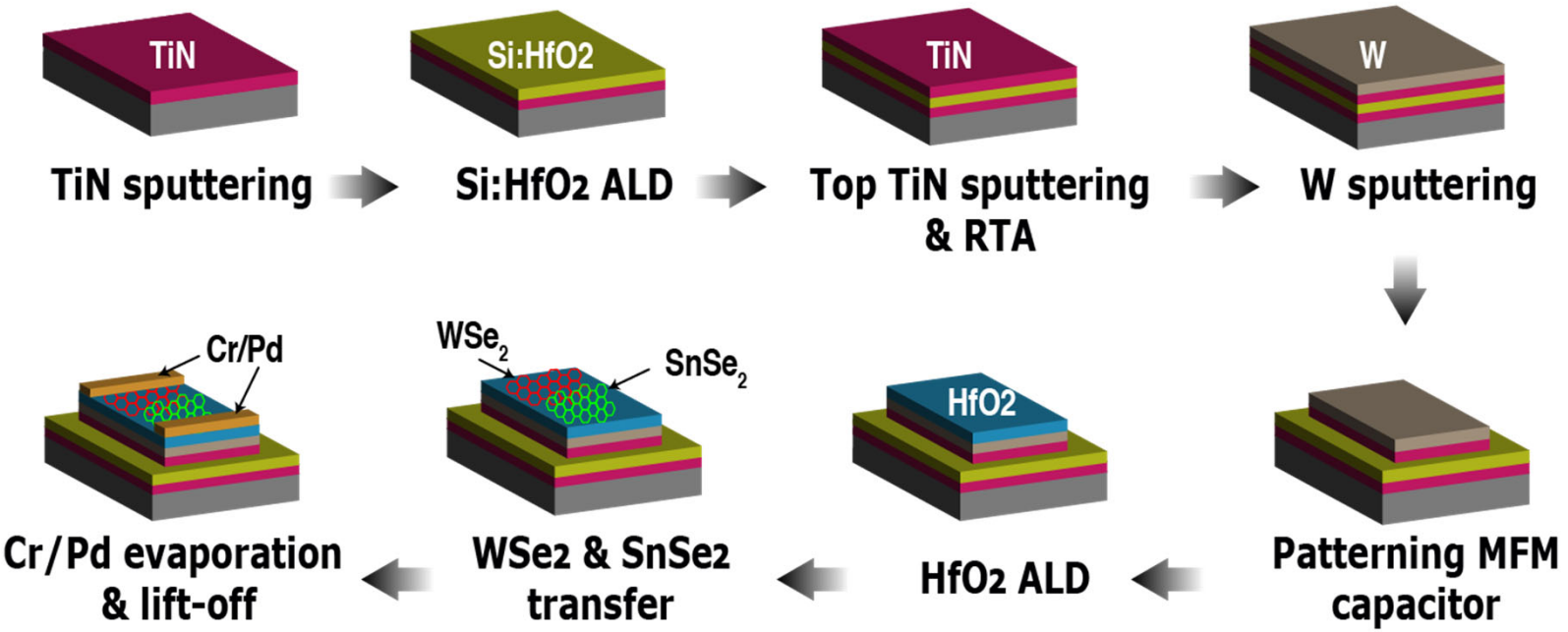
Internal gate voltage amplification
Body factor <1 and hence steeper SS

Device structure: Back-Gated $WSe_2/SnSe_2$



- Deterministic transfer **irrespective of lattice mismatch**
- **Type III,** broken-gap band alignment in **$WSe_2/SnSe_2$**: **good for tunnel FETs**

Device structure: Fabrication

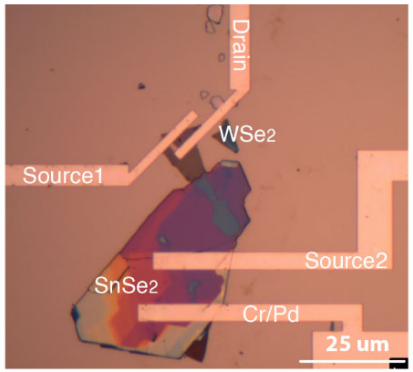


Source: S. Kamaei et al., ESSDERC 2022.

Device structure: Metrology

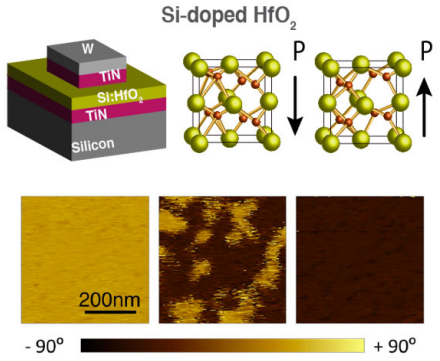
- Optical image

$WSe_2/SnSe_2$ junction, both the flakes and drain/source electrodes



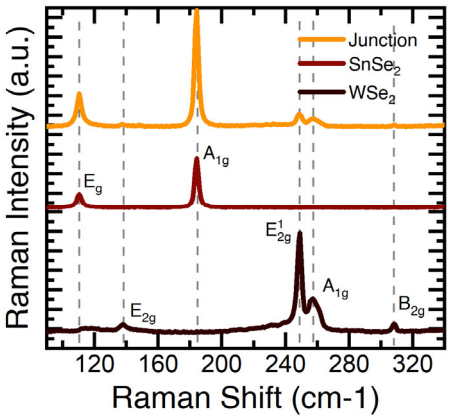
- PFM profile

Sharp and coherent polarization domain pattern, good quality FE



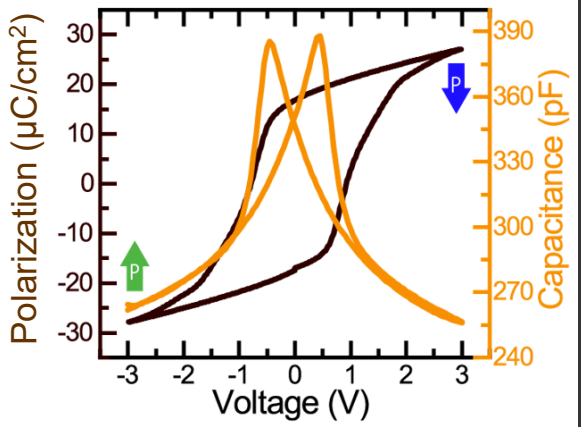
- Raman Spectrum

Identifying the peaks of both materials at the junction



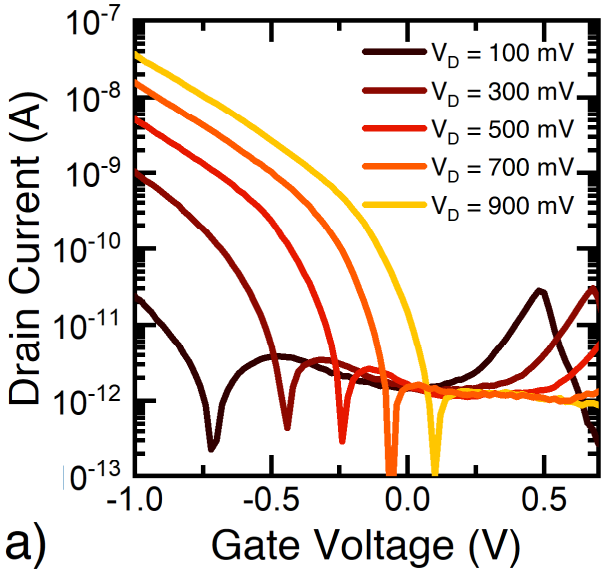
- P_V & C_V

High and uniform spontaneous polarization and low leakage conduction

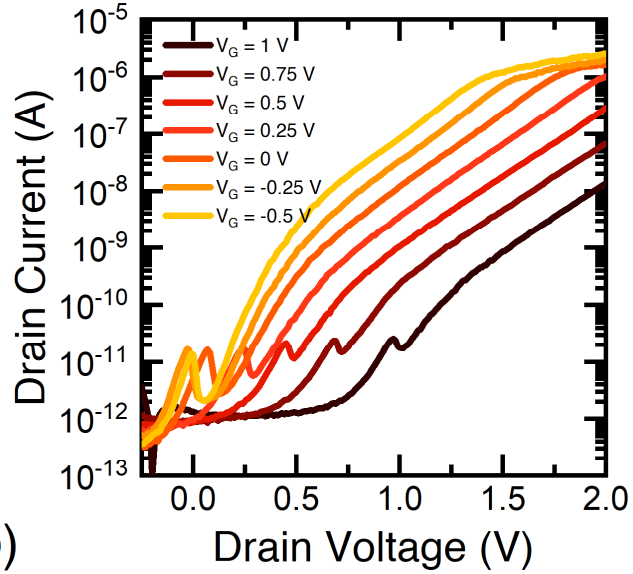


A.M. Ionescu, Negative Capacitance 2022

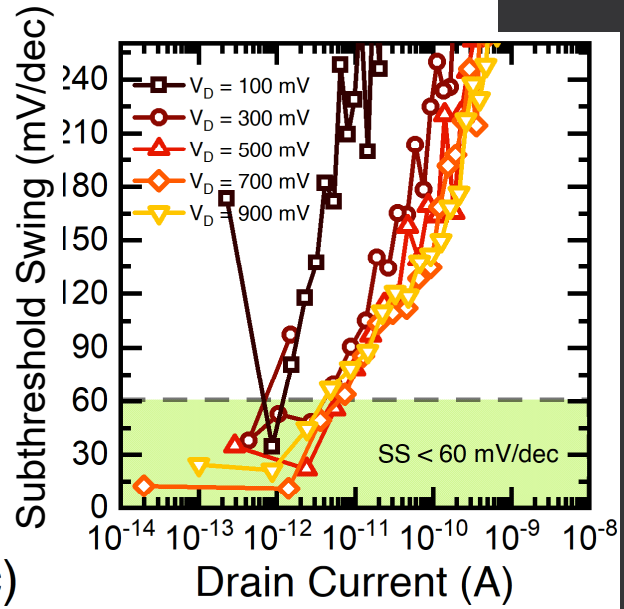
TFET characterization



a)



b)

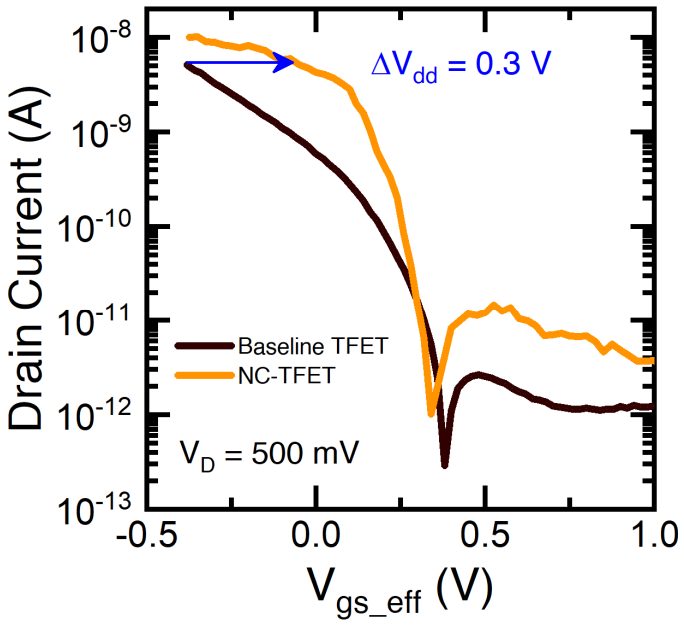


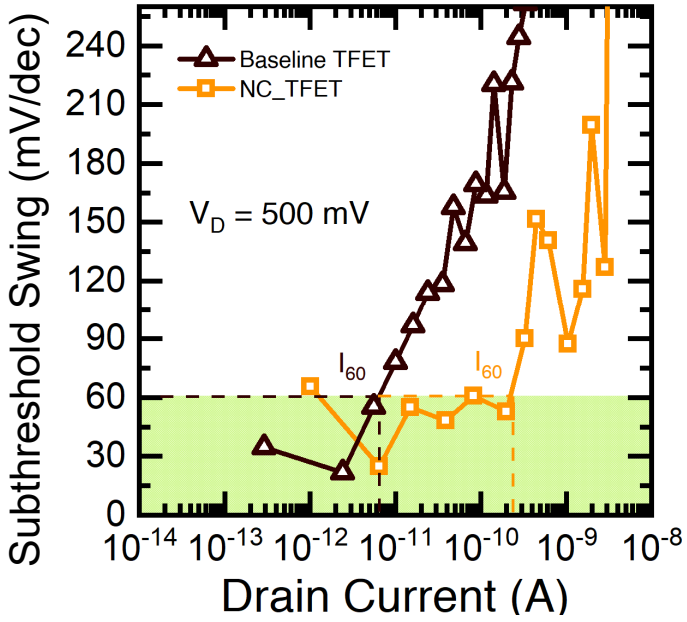
c)

- NDR tuned by gate, $I_{peak}/I_{valley} > 10$
- Subthermionic slope at room temperature
- **Sub-60 mV/dec SS** and **NDR**, **signatures of BTBT**

NC-TFET characterization

- **NC-TFET outperforms reference TFET** due to the **NC effect**

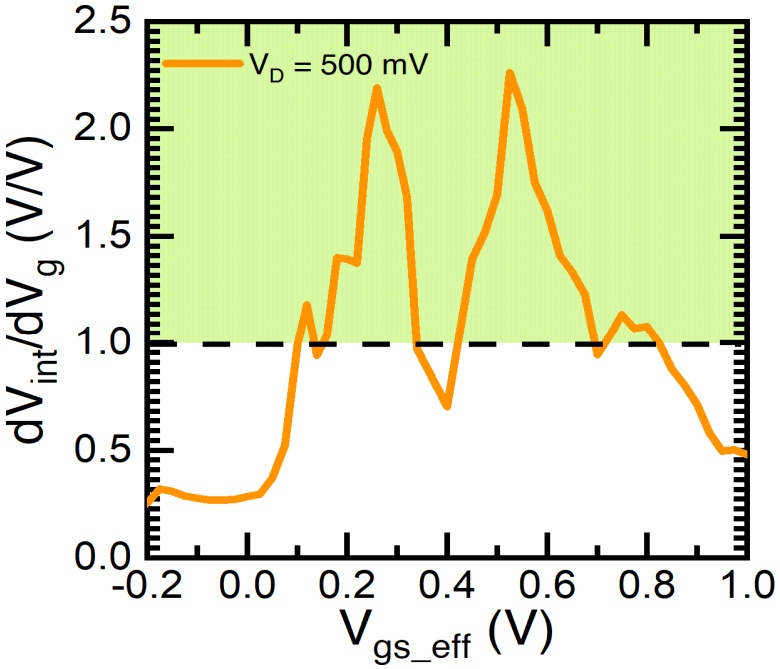




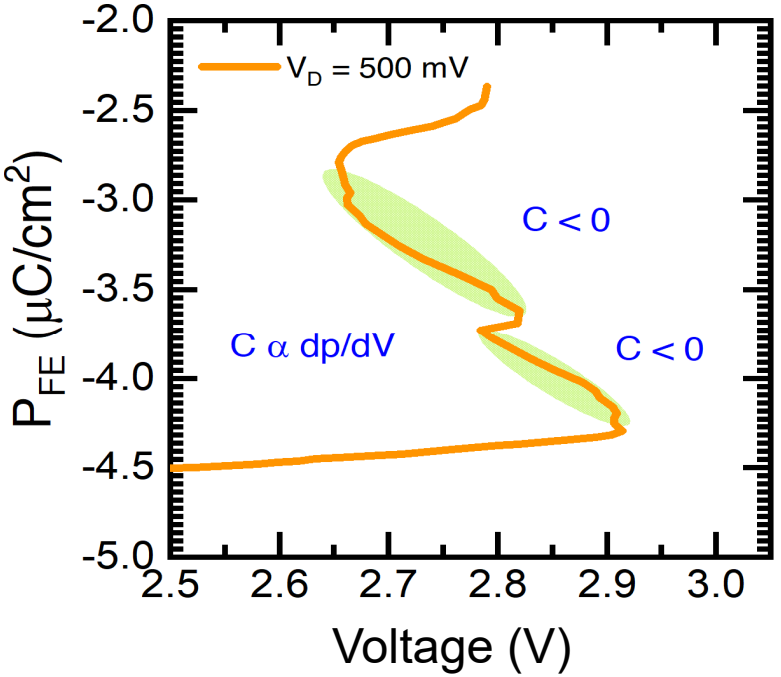
Baseline TFET
I_{60} ~ 6×10^{-6} (μA/ μm)
SS_{avg} ~ **57** mV/dec
(**2 dec of I_D**)
Sub60(dec of I_D) ~ **1.5**

NC-TFET
I_{60} ~ 2×10^{-4} (μA/ μm)
SS_{avg} ~ **56** mV/dec
(**3 dec of I_D**)
Sub-60(dec of I_D) ~ **2.5**

Evidence of NC effect

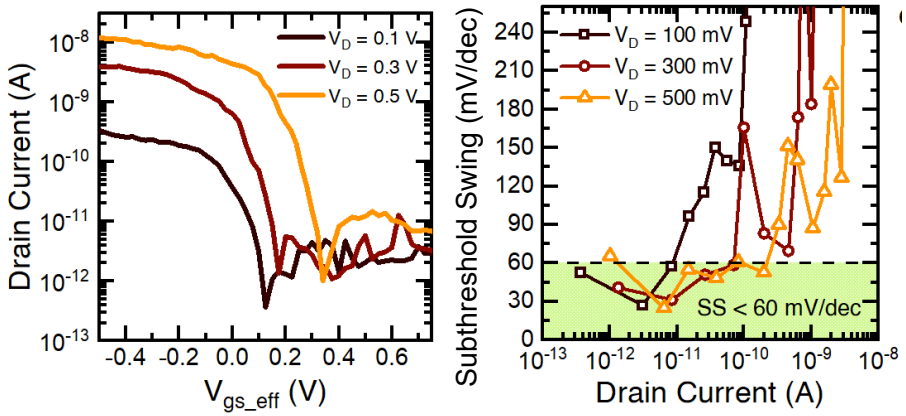


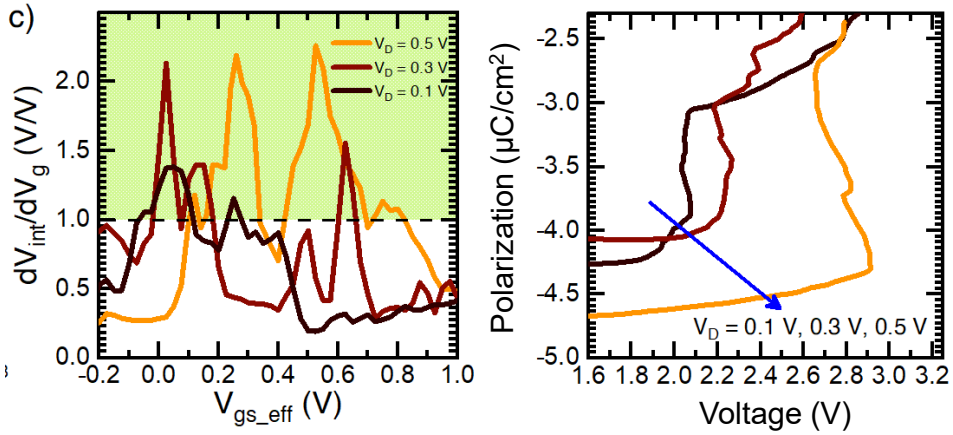
- **Voltage amplification** in the gate, **signature of NC**



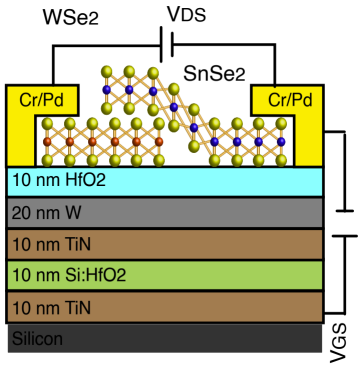
- Extracted P-V characteristic, **presence of various NC domains**

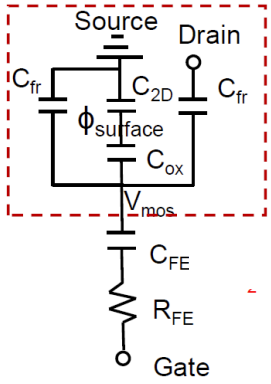
NC-TFET: effect of V_{drain}





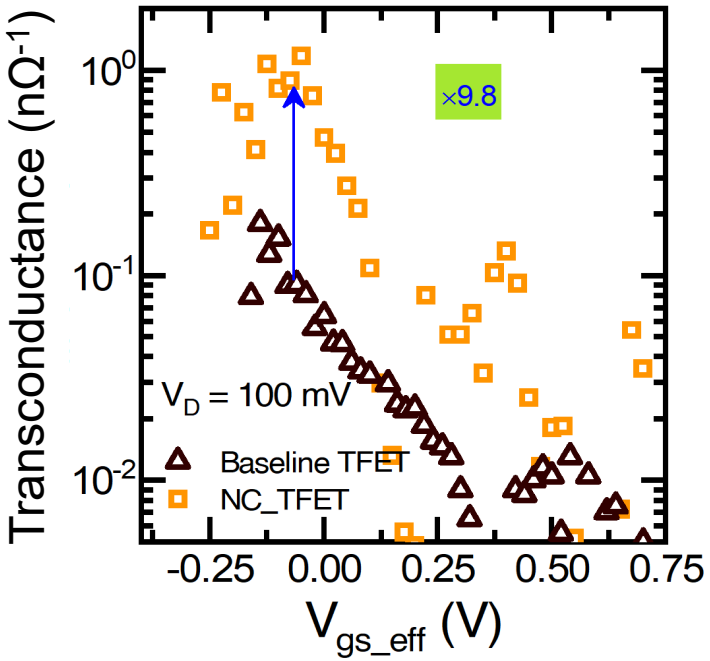
- Low SS and higher I_{on} at **higher V_D.**
- **Degradation** of *NC effect* at **lower V_D.**

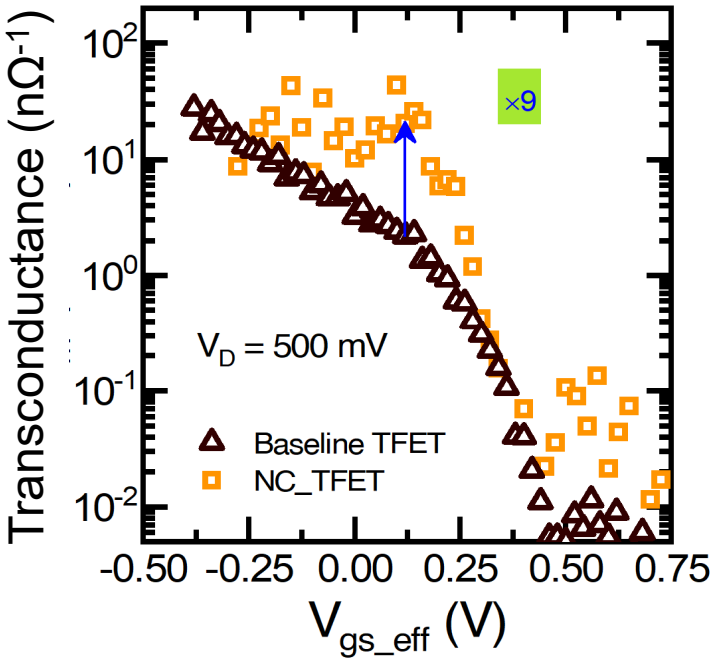




$$SS = \frac{2.3k_BT}{q} \cdot \frac{1}{\frac{\partial \phi_s}{\partial V_{gs}}} = \frac{2.3k_BT}{q}\left(1 + \frac{C_{2D}}{C_{ox}}\right) \cdot \left(1 - \frac{C_{device}}{|C_{FE}|}\right)$$

NC-TFET: Analog feature





- **NC TFET** shows **larger transconductance** than the reference Tunnel FET device at all the investigated V_D

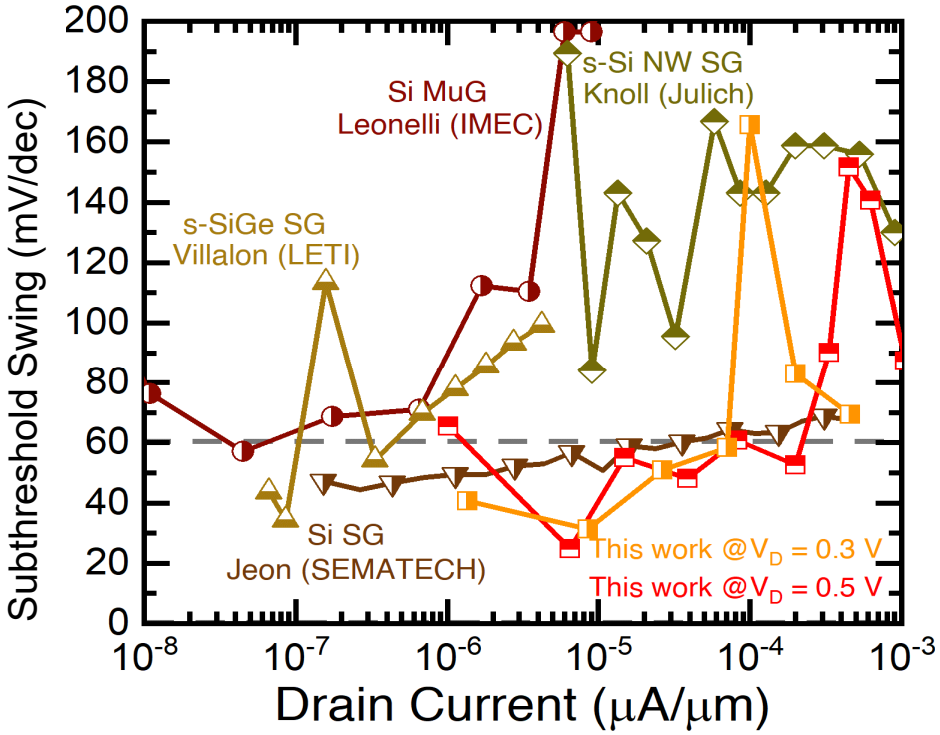
Benchmarking: EPFL's NC Tunnel FET

- **Steepest room temperature slope** SS = 24 mV/dec
- **Outperforms all previous 2D/2D TFETs** in terms of low-slope region and I_{60}

Material system	Sub-60 region (decade)	SS_{min} (mV/dec) @RT	I_{60} (µA/µm)	I_{on}/I_{off}	Ref
$WSe_2/SnSe_2$	1	35	~ 4×10^{-5}	10^5 @ V_D = 0.5 V	N. Oliva et al., IEDM, 2020
$WSe_2/SnSe_2$	~ 1	37	3×10^{-5}	10^5 @ V_D = 0.5 V	X.Yan et al., small, 2017
$MoTe_2/MoS_2$	1	34	~ 10^{-5}	10^6 @ V_D = -0.6 V	K, Bondae, et al., APL, 2018
BP/MoS_2	-	65	-	10^4 @ V_D = -0.8 V	Xu, Jiao, et al., APL, 2017
$WSe_2/SnSe_2$	-	90	-	10^6 @ V_D = 0.5 V	S.Fan et al., ACS, 2019
NC + $WSe_2/SnSe_2$	**2.3**	**24**	**2×10^{-4}**	**> 10^4 @ V_D = 0.5 V**	**This work**

Performance comparison of EPFL's NC TFET with recently reported 2D/2D TFETs

Benchmarking: SS vs. I_D

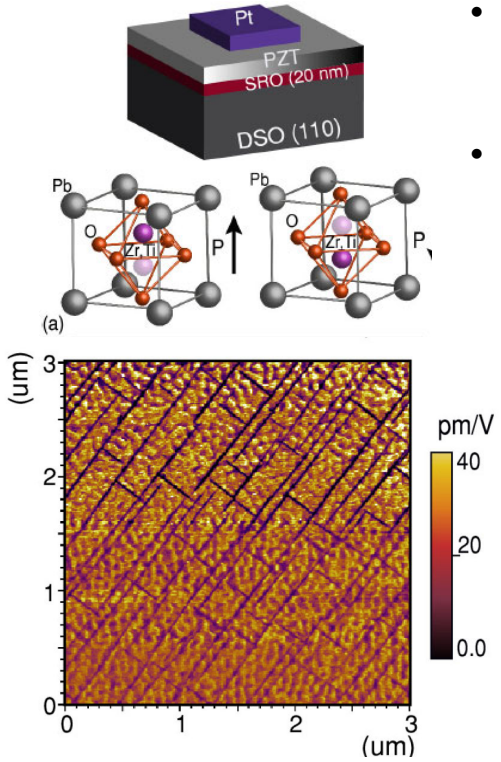


This work =
S. Kamaei et al, ESSDERC 2022.

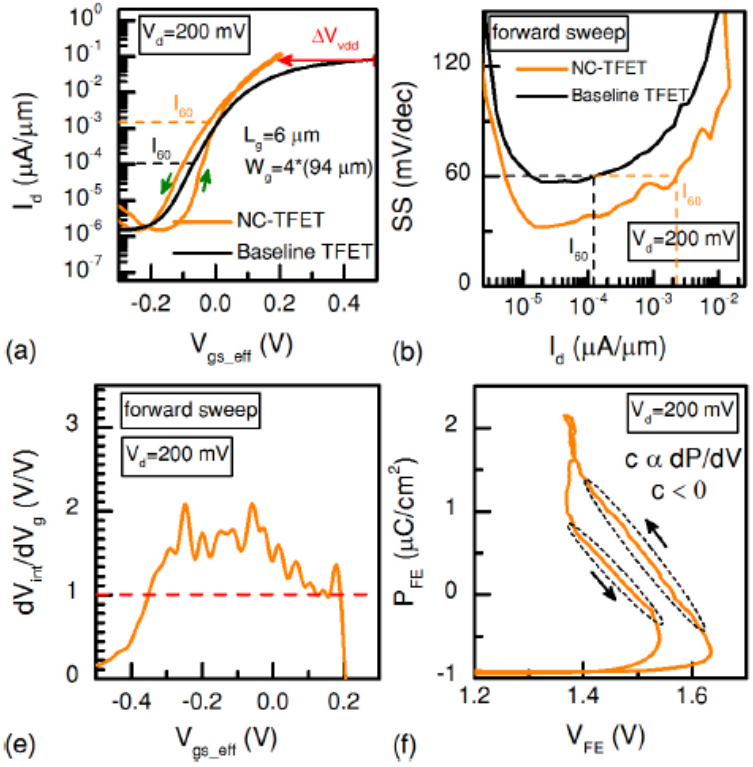
- EPFL's **2D/2D Tunnel FET device** shows **promising performance** compared to any other **p-type TFET** technologies.

(Near) Hysteresis-Free Negative Capacitance (PZT) InGaAs Tunnel FETs

Mono-crystalline PZT: no voltage training needed!

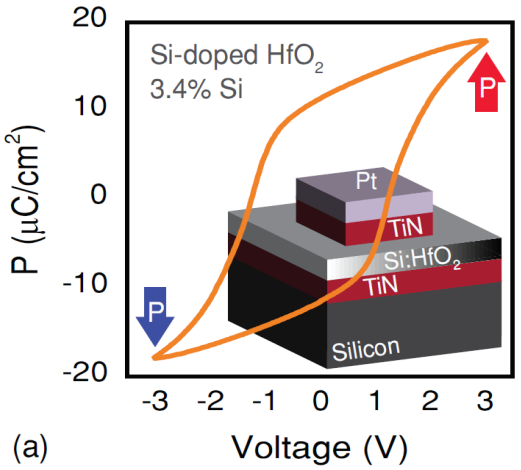


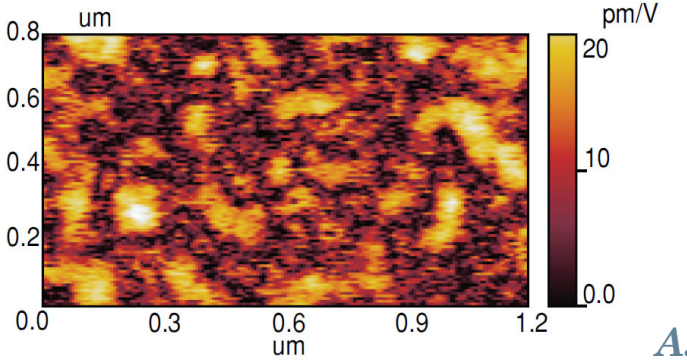
- 46nm of PZT grown on a (110) DyScO3 (DSO) substrate
- 20 nm SrRuO3 (SRO) layer as bottom electrode



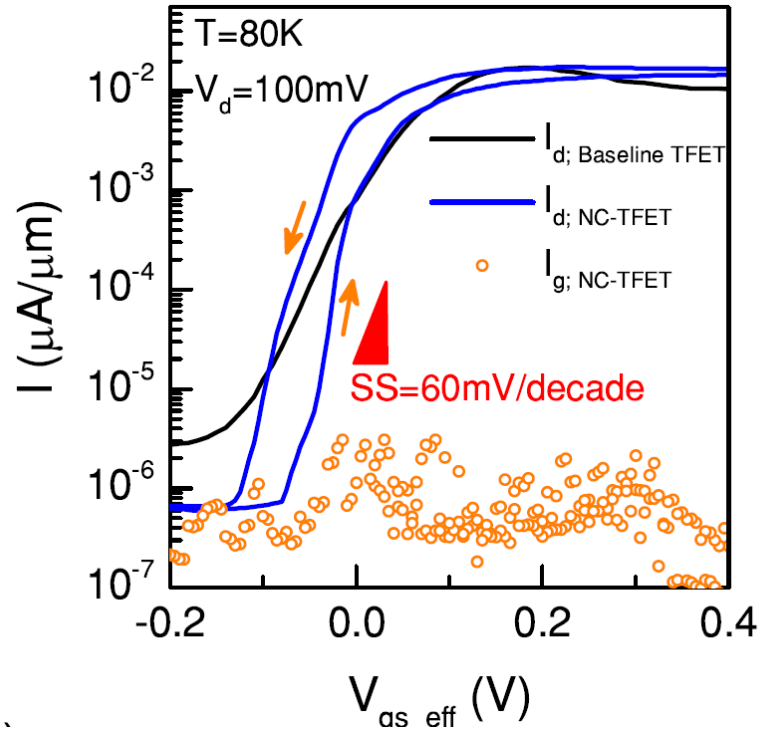
EPFL + IMEC: non-hysteretic improved results with PZT and Si-doped HfO2 @ IEDM 2018

Negative Capacitance Si:HfO2 InGaAs Tunnel FETs





- Low T suppresses TAT: only BTBT.
- STFET = 54mV/dec, SNCTFET=15mV/dec



A. Saeidi et al., to appear, 2018.

Conclusions

- Negative capacitance stands as **a performance and additive technology booster at the end of the CMOS roadmap** (applicable down to 2nm).
- It equally **applies to n- and p-type MOSFETs** with same/similar ferroelectric gate stacks.
- **Ferroelectricity (NC) in doped high-k dielectrics seem most promising integration path**; NC in PZT is a very useful experimental vehicle
- Majority of reported data is in static regime; **more dynamic experimental data is needed**.
- Negative capacitance is **a very beneficial performance booster for tunnel FETs, it improves both swing and overdrive.**
- **NC improves both digital and analog figures of merit**; therefore, of interest for low power IoT sensor nodes.